PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 5 : H01L 33/00, 21/308 — A1

(11) International Publication Number: WO 94/00885

(43) International Publication Date: 6 January 1994 (06.01.94)

(21) International Application Number: PCT/GB93/01316

(22) International Filing Date: 22 June 1993 (22.06.93)

(30) Priority data:
9213824.7 30 June 1992 (30.06.92) GB

(71) Applicant *(for all designated States except US)*: ISIS INNOVATION LTD. [GB/GB]; University Offices, Wellington Square, Oxford OX1 2JD (GB).

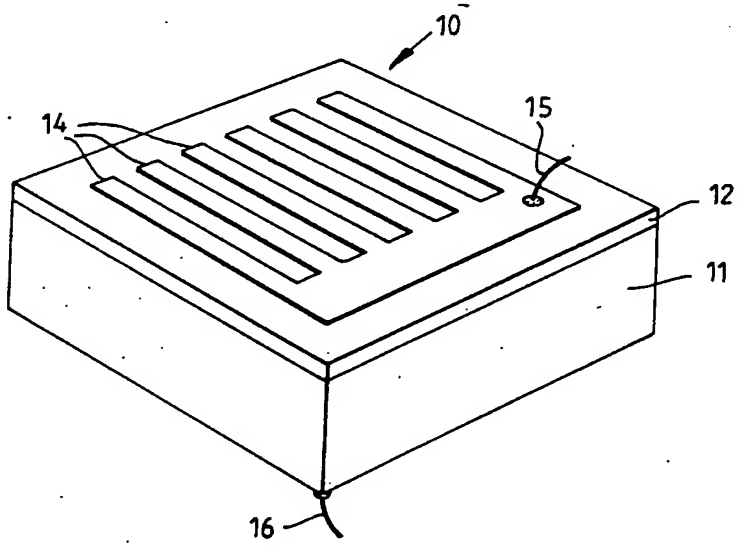
(72) Inventors; and
(75) Inventors/Applicants *(for US only)* : DOBSON, Peter, James [GB/GB]; 92 Lansdale Road, Oxford OX2 7ER (GB). LEIGH, Peter, Alexander [GB/GB]; 11 Hurst Lane, Freeland, Oxford OX8 8JA (GB). PEARSON, Robert, Owen [GB/GB]; 2 Homestead Road, London SW6 7DB (GB).

(74) Agent: BECKHAM, Robert, William; Intellectual Property Department, Defence Research Agency, R69 Building, DRA Farnborough, Hants GU14 6TD (GB).

(81) Designated States: CA, GB, JP, KR, US, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.

(54) Title: LIGHT EMITTING DEVICE



(57) Abstract

A light emitting device (10) incorporates a layer (12) of porous silicon of low dimensionality surmounted by a discontinuous layer of silver in the form of discrete islands (20). A digitated electrode (13) is connected to the islands (20). The islands (20) have diameters in the range 5nm to 20nm and spacings in the range 10nm to 50nm, and they form a Schottky diode structure on the silicon (12). Under electrical bias, the diode structure conducts and light is generated. The device (10) is produced by vacuum deposition of silver on to a silicon wafer at a temperature which provides for the silver to separate into individual balls (20). The wafer is then anodised to produce a porous layer incorporating columns of silicon and silicon dioxide surmounted by respective silver islands (20). Each silver island (20) protects the underlying silicon (21) from the anodising medium, and subsequently provides an electrical contact to the silicon.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AT	Austria
AU	Australia
BB	Barbados
BE	Belgium
BF	Burkina Faso
BG	Bulgaria
BJ	Benin
BR	Brazil
BY	Belarus
CA	Canada
CF	Central African Republic
CG	Congo
CH	Switzerland
CI	Côte d'Ivoire
CM	Cameroon
CN	China
CS	Czechoslovakia
CZ	Czech Republic
DE	Germany
DK	Denmark
ES	Spain
FI	Finland
FR	France
GA	Gabon
GB	United Kingdom
GN	Guinea
GR	Greece
HU	Hungary
IE	Ireland
IT	Italy
JP	Japan
KP	Democratic People's Republic of Korea
KR	Republic of Korea
KZ	Kazakhstan
LI	Liechtenstein
LK	Sri Lanka
LU	Luxembourg
LV	Latvia
MC	Monaco
MG	Madagascar
ML	Mali
MN	Mongolia
MR	Mauritania
MW	Malawi
NE	Niger
NL	Netherlands
NO	Norway
NZ	New Zealand
PL	Poland
PT	Portugal
RO	Romania
RU	Russian Federation
SD	Sudan
SE	Sweden
SI	Slovenia
SK	Slovak Republic
SN	Senegal
TD	Chad
TG	Togo
UA	Ukraine
US	United States of America
UZ	Uzbekistan
VN	Viet Nam

LIGHT EMITTING DEVICE

This invention relates to a light emitting device and to a method of making such a device. The invention is particularly directed to a device which employs luminescent semiconductor properties.

There has been much research recently into visible electroluminescence from porous silicon, which is a sponge-like structure made by first anodising and then etching a silicon substrate. Three papers which discuss the present state of the art are as follows: L T Canham, "Silicon Quantum wire array fabrication by electrochemical and chemical dissolution of wafers"; Appl. Phys. Lett. 57 (10), 3rd September 1990, page 1046; Nobuyoshi Koshida and Hideki Koyama,, "Visible electroluminescence from porous silicon", Appl. Phys. Lett. 60 (3), 20th January 1992, page 347; and Volker Lehman and Ulrich Gösele, "Porous Silicon: Quantum sponge structures grown via a self-adjusting etching process", Adv. Mater. 4 (1992) No. 2, page 114.

The basic prior art light emitting device is disclosed in the aforementioned paper by Koshida and Koyama. It consists of a diode structure made from a substrate of p-type silicon, on top of which is formed a porous layer, typically 0.2 μm to 1.0 μm thick. Electrodes are placed both on the porous layer and on the underside of the substrate so that an electrical bias potential can be applied to the diode. One of the electrodes, that on the porous layer, is made of semi-transparent material so that light generated within the diode structure may be emitted.

The porous layer is formed by subjecting the top surface of the substrate to anodisation. This is believed to produce a porous layer comprising an array of columns or wires of low dimensionality, vertical to the surface, and separated by holes or spaces and wherein each column comprises silicon embedded in silicon oxide. Generally the porosity of the layer is increased by subsequent etching. An etchant is used which thins the columns by chemical dissolution, with a resultant increase in the size of the spaces between the columns. Light is generated within the diode

structure in response to electrical bias. There is currently some uncertainty in the scientific world as to how the structure emits light.

The present invention provides a light emitting device incorporating porous material of low dimensionality consisting at least partly of semiconductor material and produced by an etching process, upon the porous material a discontinuous layer comprising islands of electrically conducting and etch resistant material, together with contacting means for making electrical contact to the porous material and the discontinuous layer.

The expression "low dimensionality" in relation to a material means that the material has, in at least one direction, dimensions of the order of or less than the exciton diameter or the De Broglie wavelength of electrons or holes in the material. This leads to quantum confinement in the relevant direction. Quantum wells, quantum wires and quantum dots are known in the prior art and correspond to one, two and three dimensional confinement respectively. In practice, this corresponds to material feature dimensions less than 50nm in extent, and preferably less than 25nm.

The invention provides the advantage that it is a light emitting semiconductor device which is activated by electrical bias applied to the contacting means.

The invention also provides the advantage that the residual semiconductor material remaining in the porous layer is that located under the islands of electrically conducting and etch resistant material, which provided protection thereof during the etching process. The islands therefore define the locations of residual semiconductor material, and provide electrical contact to resulting low dimensional semiconductor material. The islands may have diameters of 5nm to 100nm, preferably 5nm to 20nm or 10nm to 20nm, and inter-island spacings may be in the range 10nm to 500nm, preferably 10nm to 50nm.

The semiconductor material is preferably silicon, and the electrically conducting and etch resistant material is preferably silver forming a Schottky diode structure with the silicon. An embodiment of the invention in which the semiconductor material is silicon and the etch resistant material is silver has produced orange electroluminescence emission in response to electrical bias in the range 7 to 9 volts applied to the contacting means. This range of bias produced current densities in the range 100 to 200 $mAcm^{-2}$.

The contacting means may include a digitated electrode connected to islands of electrically conducting and etch resistant material.

In an alternative aspect, the invention provides a light emitting device incorporating porous material of low dimensionality comprising columns consisting at least partly of semiconductor material tipped with electrically conducting material, and contacting means for making electrical contact to the porous material and to the electrically conducting material.

In a further aspect, the invention provides a method of making a light emitting device including the steps of:-

(a) forming a discontinuous layer of islands of electrically conducting and etch resistant material upon semiconductor material,

(b) anodising the semiconductor material to produce a porous region consisting at least partly of semiconductor material of low dimensionality and protected from anodisation by the electrically conducting and etch resistant material, and

(c) providing electrical connections to the semiconductor material and to the electrically conducting and etch resistant material respectively.

The islands may be 5nm to 100nm (preferably 5nm to 20nm or 10nm to 20nm) in diameter and may have spacings in the range 10nm, to 100nm, (preferably 10nm to 50nm); they may be distributed in either a random manner or a regular manner on the semiconductor material. Preferably the islands are of metallic material such as silver.

The islands define those regions of the silicon surface which are protected from being anodically attacked, and thus they define the structure of the porous silicon layer in addition to providing electrical contact thereto. Silver is the preferred island material, since it forms a good Schottky barrier to silicon semiconductor material, thus providing a diode structure.

The porous layer may be etched after anodisation.

Electrical connections may be made to islands to form one electrical bias terminal of the device. A second bias terminal may be provided by making an ohmic contact to a side of the semiconductor material remote from the porous layer. The electrical connection to the islands may be formed by depositing a second layer of electrically conducting material such as silver to connect islands together to form an electrically continuous layer. Preferably this second layer is of digitated form, having fingers connecting the islands, and exposing areas of the porous layer between the fingers.

In order that the invention might be more fully understood, an embodiment thereof will now be described, by way of example only and with reference to the accompanying drawings, in which:-

Figure 1 is a diagrammatic side view of a prior art light emitting device;

Figure 2 is a schematic perspective view of a light emitting device of the invention;

Figures 3 and 4 schematically illustrate two successive steps in manufacture of the device of Figure 2;

Figure 5 is a schematic drawing of columns of silicon/silicon dioxide in a device of the invention; and

Figure 6 shows the electronic band structure of the device partly shown in Figure 5.

Referring to Figure 1, this illustrates a prior art diode structure as described by Koshida et al previously referred to. It has a substrate 1 of p-type silicon, on top of which is formed a porous layer 2, typically 0.2-1.0μm thick. Electrodes 3 and 4 are placed on the porous layer 2, and on the underside of the substrate 1 so that suitable potentials can be applied via respective terminals 5,6. Electrode 3, on the porous layer, is made of semi-transparent material so that light generated within the structure may be emitted.

The porous layer 2 is formed by subjecting the top surface of the substrate 1 to anodisation, typically in hydrofluoric acid (HF) and ethanol, and at low moderate current densities, typically 10 mA/cm^2, for 5 to 10 minutes. The anodisation is believed to produce a porous layer 2 which is a low dimensional structure having quantum confinement properties as discussed in the prior art. It comprises an array of columns or wires, vertical to the surface, and separated by holes or spaces and wherein each column comprises silicon embedded in silicon oxide. Generally, the porosity of layer 2 is increased by subsequent etching, using an etchant which thins the columns by chemical dissolution, typically to sizes less than 10nm wide, with a resultant increase in the size of the spaces between the columns.

It is found that, under the correct circumstances, application of a d.c. source to the structure shown in Figure 1, and with a negative potential on the electrode 3 and a positive potential on the electrode 4, can result in light being generated within the structure. There is currently some

uncertainty in the scientific world as to how the silicon emits light, but the exact mechanism is not of relevance as far as concerns the present invention. However, as will be described later in more detail in relation to the invention, it is believed that luminescence emission arises from recombination of quantum confined charge carriers.

Although references are made herein solely to silicon, there is evidence that other semiconductor materials, such as germanium, gallium arsenide and other compound semiconductors also exhibit quantum confinement effects. The specification should be construed accordingly.

Referring to Figure 2, there is shown a light emitting device of the invention indicated generally by 10. It comprises a substrate 11 of p-type silicon on top of which, by a method to be described, is formed a layer 12 of porous silicon. Formed on the porous silicon layer 12 is a digitated electrode 13 having fingers, such as 14, of silver. In one manifestation the grating pitch of the electrode fingers, 14 is chosen to select and/or enhance the emitted light, and is in the range 0.5μm to 1μm. In other manifestations, the fingers 19 would have a width in the range 2μm to 10μm and a centre to centre pitch of 4μm to 10μm. A typical overall size of electrode 18 would be in the range of 0.1mm to 1mm square, and the mean thickness of the electrode silver would be in the range 10nm to 20nm.

A plain ohmic contact electrode (not visible) is formed on the undersurface of the substrate 11. Terminals 15 and 16 enable electrical connections to be made to the electrode 13 and ohmic contact respectively.

Referring now to Figures 3 and 4, in which parts previously described are like-referenced, there are illustrated steps in the method of making the device 10. It is to be emphasised that both Figures 3 and 4 are highly schematic and are not to scale.

The process commences by forming on one of the surfaces of the silicon substrate 11 the layer 12 of porous silicon. This is achieved by

anodisation of the surface in any known manner, for example as in the prior art, and optionally by subsequent etching of the surface using a suitable chemical etchant. Prior to anodisation, however, the surface is formed with an array of spots or islands 20 of conductive material, preferably silver. The islands may be of irregular shape, but are preferably generally circular. Typical island sizes range from 5nm or 10nm to 20nm diameter and typical spacing between islands is in the range 10nm to 50nm. The islands may be irregularly positioned, but preferably they are formed in an ordered array.

The islands 20 are formed by vacuum depositing silver onto the surface of a clean silicon wafer held, typically, at between 300 and 400°K in such a manner that it forms a discontinuous island film. It is known that thin film deposition of low melting point metals such as silver onto dielectrics such as Si/SiO_2 results in an island deposit. This is because of the tendency of a system to minimise its free energy; i.e. because the silver/silica bond is not strong, the silver does not wet the silica, and it tends to ball up and form discrete hemispherical islands. If silver deposition is terminated at around 1nm to 5nm average thickness at 300°K, silver islands in the range 5nm to 20nm in diameter would be expected, but with a wide variety of separations. Island diameters in the range 10-100nm could be employed, with inter-island separations in the range 10-500nm.

Islands 20 define regions of the silicon wafer 11 where anodisation does not occur by protecting the regions underlying the islands from attack. The result is that the anodised layer takes up a structure somewhat similar to that illustrated in Figure 4 in which isolated columns 21 of silicon underlie the islands and are upstanding from the substrate 11.

Subsequent etching, if required, using a chemical etchant will further define the device structure, and increase the pore size of the porous silicon layer 12 to the desired extent. The islands 20 maintain their protection of the underlying silicon during etching.

Electron microscopy of porous silicon produced as described above has shown small crystallites of silicon and large platelets of an unidentified single crystal phase.

The next stage is to link the islands 20 electrically to form an electrical connection. This is achieved in the described embodiment by forming on the top surface of the structure illustrated in Figure 4 the digitated electrode structure 13 shown in Figure 2. This may be achieved by a second silver deposition.

Finally a first ohmic connection 16 is made to the underside of the silicon substrate 11 and a second connection 15 to the electrode 13, so than an appropriate source (not shown) of electrical bias potential may be applied between the connections 15 and 16.

The device 10 shown in Figure 2 forms a Schottky diode; upon application of a negative pole of an electrical potential source to the terminal 15 and a positive pole of that source to the terminal 16, the device 10 will be forward biased and will conduct in the manner of a diode. If however, n-type silicon were to be used for the substrate 11, these potentials should be reversed.

During conduction through the device 10, light is generated, which is believed to come from the porous silicon layer 12. The formation of columns 21 of silicon ensure that the optimum electric field is produced in the vicinity of the porous layer 12. In addition, a benefit of using silver is that there is an electromagnetic enhancement effect with silver due to the excitation of surface plasmons. The use of a digitated structure for the electrode 13 improves the distribution of generated light over the device 10, since, in operation, the current density within the porous layer 12 is higher at the electrode edges, giving an edge emission effect.

One embodiment of the device 10 was subjected to an electrical bias voltage in the range 7 to 9 volts applied across the connections

15 and 16. This resulted in a current density in the range 100-200 $mAcm^{-2}$ flowing in the device 10. Orange electroluminescence emission was clearly observed from the device 10. The emission was localised at edges and holes in the electrode 13.

Whereas silver has a number of meritorious properties rendering it suitable for use in the invention, it suffers from the disadvantage of having a tendency to diffuse in a porous structure. It would therefore be advantageous to provide an alternative island and/or electrode material which exhibited the meritorious properties of silver but had lower diffusion characteristics. Silicide compounds are possible candidates for this.

In order to facilitate formation of the electrode 13 and its connection to the islands 20, it is possible to fill the pores of the porous layer 12 with an inert material providing a planar surface at the level of the islands 20. The inert material should be an insulating dielectric, eg a polymer such as polymethylmethacrycrate, polyethylene or polytetrafluoroethylene. The polymer may be introduced into the porous layer 12 in solution, and subsequently baked to remove solvent. Alternatively, a monomer may be used to fill the porous layer pores and subsequently polymerised in situ chemically or using ultra-violet light. Subsequently, excess polymer may be removed by etching or polishing to expose the islands 20 in a polymer surface. An electrode may then be deposited on the polymer surface to contact the islands 20.

As already mentioned, there is currently some uncertainty as to the mechanism of electroluminescence in porous silicon structures, and the invention is not to be construed as being restricted to any particular mechanism. However, it is believed that anodisation and etching results in small regions of silicon being left encapsulated in porous silicon oxide. If anodising and etching is carried out in such a way as to structure the silicon as a chain of individual beads, typically of 1nm to 10nm in size, encapsulated within the silicon oxide, then these beads can act as quantum particles which can be excited into luminescence. In

such a structure, luminescence in the quantum particles would be excited by positive holes tunnelling via the porous silicon from the p-type substrate on their way to the negative metal electrode.

Other possible mechanisms are:

(a) Quantum wire structures, as described by Canham (see above),

(b) Amorphised silicon - this is a known red/orange emitter and the anodising/etching may act to render the surface region amorphous;

(c) A siloxene compound - SiOxHy - which is luminescent, is formed by the anodising and etching.

Referring now to Figure 5, there is shown a schematic drawing of a possible structure 30 of silicon material produced in accordance with the invention. The structure 30 consists of what are referred to as "beads" of silicon 31 connected by regions 32 to form columns 33 surmounted by respective metal islands such as 34. The regions 32 are of SiO_2 dielectric material. The beads 31 and regions 32 are of varying sizes. The columns 33 are embedded in a matrix, indicated by lines 35, of porous SiO_2; ie the matrix 35 is part SiO_2, part void.

Referring now also to Figure 6, in which parts described earlier are like referenced, there is shown a schematic drawing of the band structure 40 of the structure 30 under an applied electrical bias voltage V_{bias}. It is assumed that the structure 30 was produced from a p type silicon substrate as indicated at 41. Quantum confinement occurs in the silicon beads 31 between wider band gap SiO_2 regions 32, as indicated by energy levels such as 42. Since the beads 31 are of varying size, the bound states within them are of varying energies; beads of lesser and greater thicknesses correspond to higher and lower energy states respectively. The SiO_2 regions 32 are very thin, and an electron within an Si bead may either tunnel through an adjacent SiO_2 region or recombine with a hole within the

same bead. Tunnelling between Si beads results in electrons and holes occupying a range of energy states which are related to the dimensions and shape of the respective bead in each case. Subsequent recombination produces a range of luminescent wavelengths.

It is advantageous to employ a Schottky diode structure in devices of the invention. This is because, as illustrated in Figure 6, bending of valence and conduction bands at and near a semiconductor surface is reduced by the presence of the metal component of the barrier. A high degree of band bending has the effect of reducing electroluminescence emission.

CLAIMS

1. A light emitting device incorporating porous material of low dimensionality consisting at least partly of semiconductor material and produced by an etching process, upon the porous material a discontinuous layer comprising islands of electrically conducting and etch resistant material, together with contacting means for making electrical contact to the porous material and the discontinuous layer.

2. A device according to Claim 1 wherein the islands have diameters in the range 5nm to 100nm.

3. A device according to Claim 2 wherein the islands have diameters in the range 5nm to 20nm.

4. A device according to Claim 3 wherein the islands have diameters in the range 10nm to 20nm.

5. A device according to Claims 1, 2, 3 or 4 wherein the islands have spacings therebetween in the range 10nm to 100nm.

6. A device according to Claim 5 wherein the islands have spacings therebetween in the range 10nm to 50nm.

7. A device according to any preceding claim wherein the semiconductor material is silicon.

8. A device according to any preceding claim wherein the semiconductor material and the electrically conducting material form a Schottky diode structure.

9. A device according to any preceding claim wherein the electrically conducting material is silver.

10. A device according to any preceding claim wherein the contacting means incorporates a digitated electrode structure connected to the electrically conducting material.

11. A device according to Claim 10 wherein the digitated electrode structure has a grating pitch arranged to select and/or enhance light emission.

12. A device according to Claim 11 wherein the grating pitch is in the range 0.5μm to 1μm.

13. A device according to Claim 10 wherein the digitated electrode structure has fingers with width in the range 2μm to 10μm and a grating pitch in the range 4μm to 20μm.

14. A light emitting device incorporating porous material of low dimensionality comprising columns consisting at least partly of semiconductor material and tipped with respective regions of electrically conducting material, and contacting means for making electrical contact to the porous material and to the electrically conducting material.

15. A device according to Claim 14 wherein the columns comprise beads of semiconductor material linked together by dielectric material.

16. A device according to Claim 14 or 15 wherein the regions have diameters in the range 5nm to 100nm.

17. A device according to Claim 16 wherein the regions have diameters in the range 5 to 20nm.

18. A device according to Claim 17 wherein the regions have diameters in the range 10nm to 20nm.

19. A device according to Claim 16, 17 or 18 wherein the regions have spacings therebetween in the range 10nm to 100nm.

20. A device according to Claim 19 wherein the regions have spacings therebetween in the range 10nm to 50nm.

21. A device according to any one of Claims 14 to 20 wherein the semiconducting material is silicon.

22. A device according to Claim 21 wherein the columns comprise silicon regions linked together by silicon dioxide regions.

23. A device according to any one of Claims 14 to 22 wherein the semiconducting material and the electrically conducting material form a Schottky diode structure.

24. A device according to any one of Claims 14 to 23 wherein the electrically conducting material is silver.

25. A device according to any one of Claims 14 to 24 wherein the contacting means incorporate a digitated electrode structure connected to the electrically conducting material.

26. A device according to Claim 25 wherein the digitated electrode structure has fingers arranged with a grating pitch to select and/or enhance light emission.

27. A device according to Claim 26 wherein the grating pitch is in the range 0.5μm to 1μm.

28. A device according to Claim 25 wherein the digitated electrode structure has fingers with width in the range 2μm to 10μm and a grating pitch in the range 4μm to 20μm.

29. A method of making a light emitting device including the steps of:-

(a) forming a discontinuous layer of islands of electrically conducting and etch resistant material upon semiconductor material,

(b) anodising the semiconductor material to produce a porous region consisting at least partly of semiconductor material of low dimensionality and protected from anodisation by the electrically conducting and etch resistant material, and

(c) providing electrical connections to the semiconductor material and to the electrically conducting and etch resistant material respectively.

30. A method according to Claim 29 wherein the islands have diameters in the range 5nm to 100nm.

31. A method according to Claim 30 wherein the islands have diameters in the range 5nm to 20nm.

32. A method according to Claim 31 wherein the islands have diameters in the range 10nm to 20nm.

33. A method according to Claim 29, 30, 31 or 32 wherein the islands have spacings therebetween in the range 10nm to 100nm.

34. A method according to Claim 33 wherein the islands have spacings therebetween in the range 10nm to 50nm.

35. A method according to any one of Claims 29 to 34 wherein the semiconductor material is silicon.

36. A method according to any one of Claims 27 to 33 wherein the electrically conducting and etch resistant material and the semiconductor material form a Schottky diode structure.

37. A method according to any one of Claims 29 to 36 including the step of connecting a digitated electrode structure to the electrically conducting and etch resistant material.

38. A method according to any one of Claims 29 to 37 wherein the islands are formed by vacuum deposition of silver on to semiconductor material maintained at a temperature appropriate to cause balling of the silver.

Fig.1

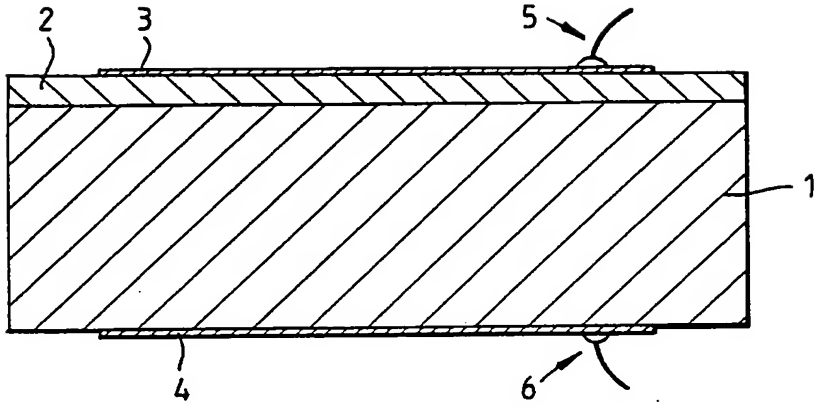


Fig.2

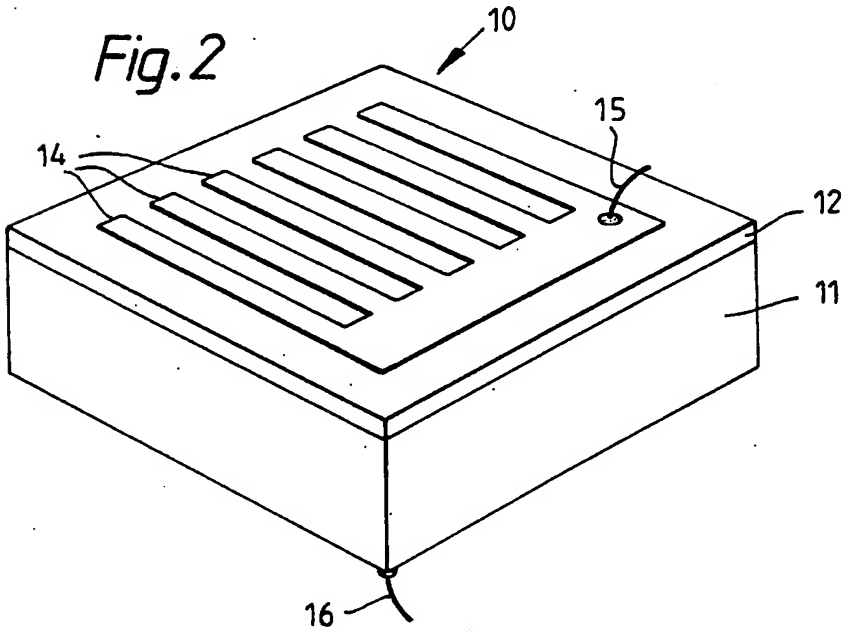


Fig.3

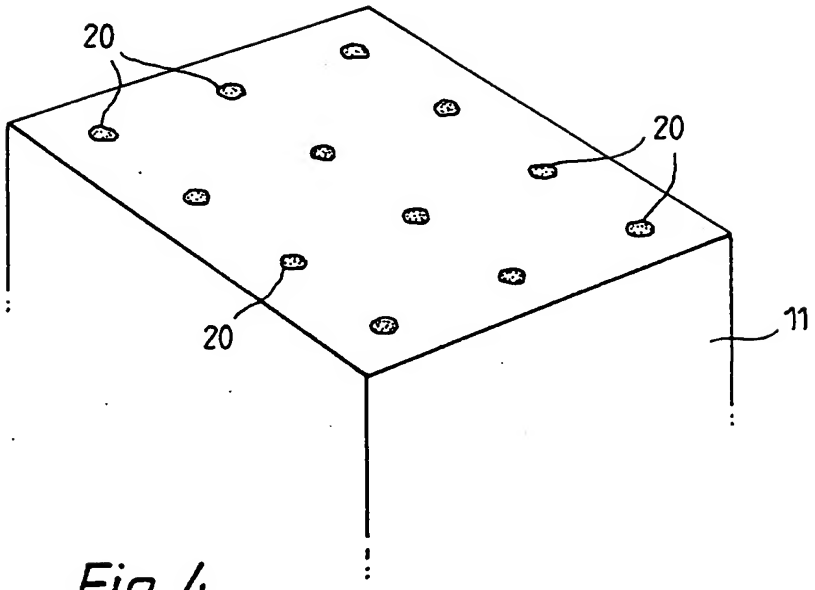


Fig.4

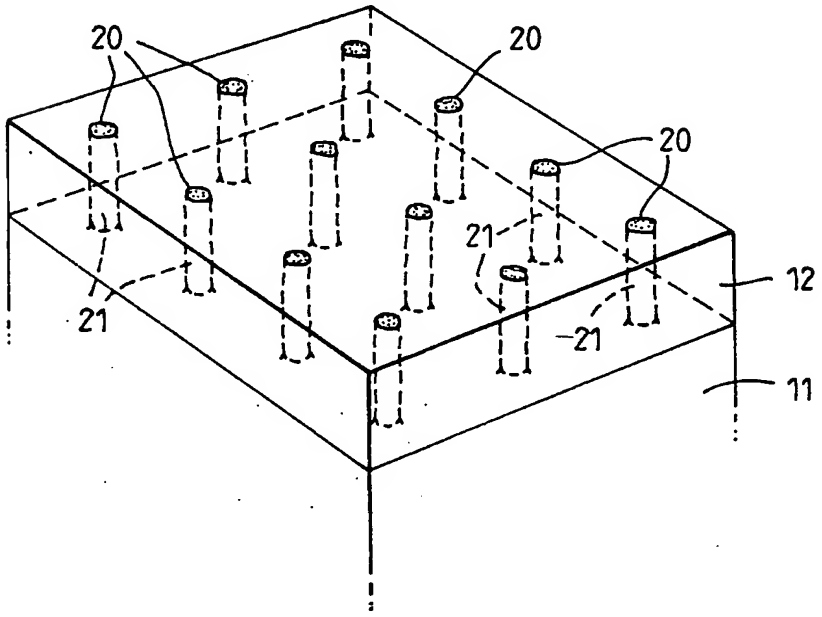


Fig. 5

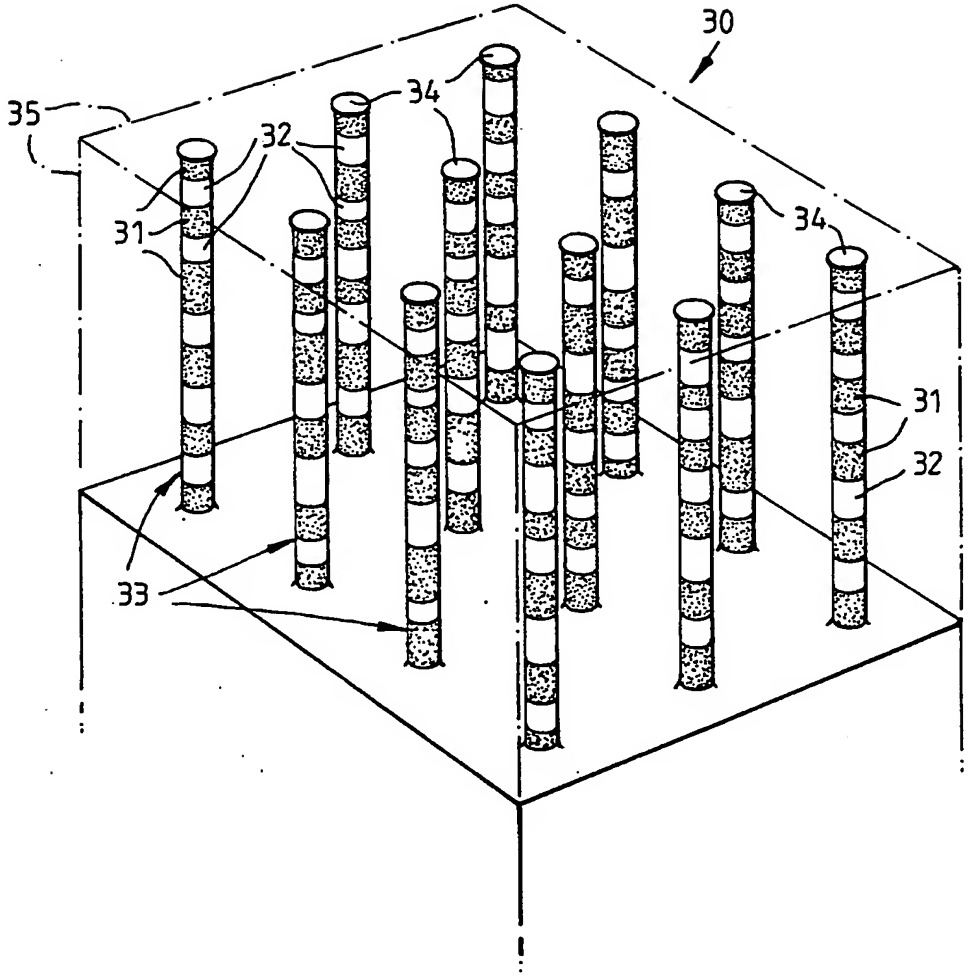
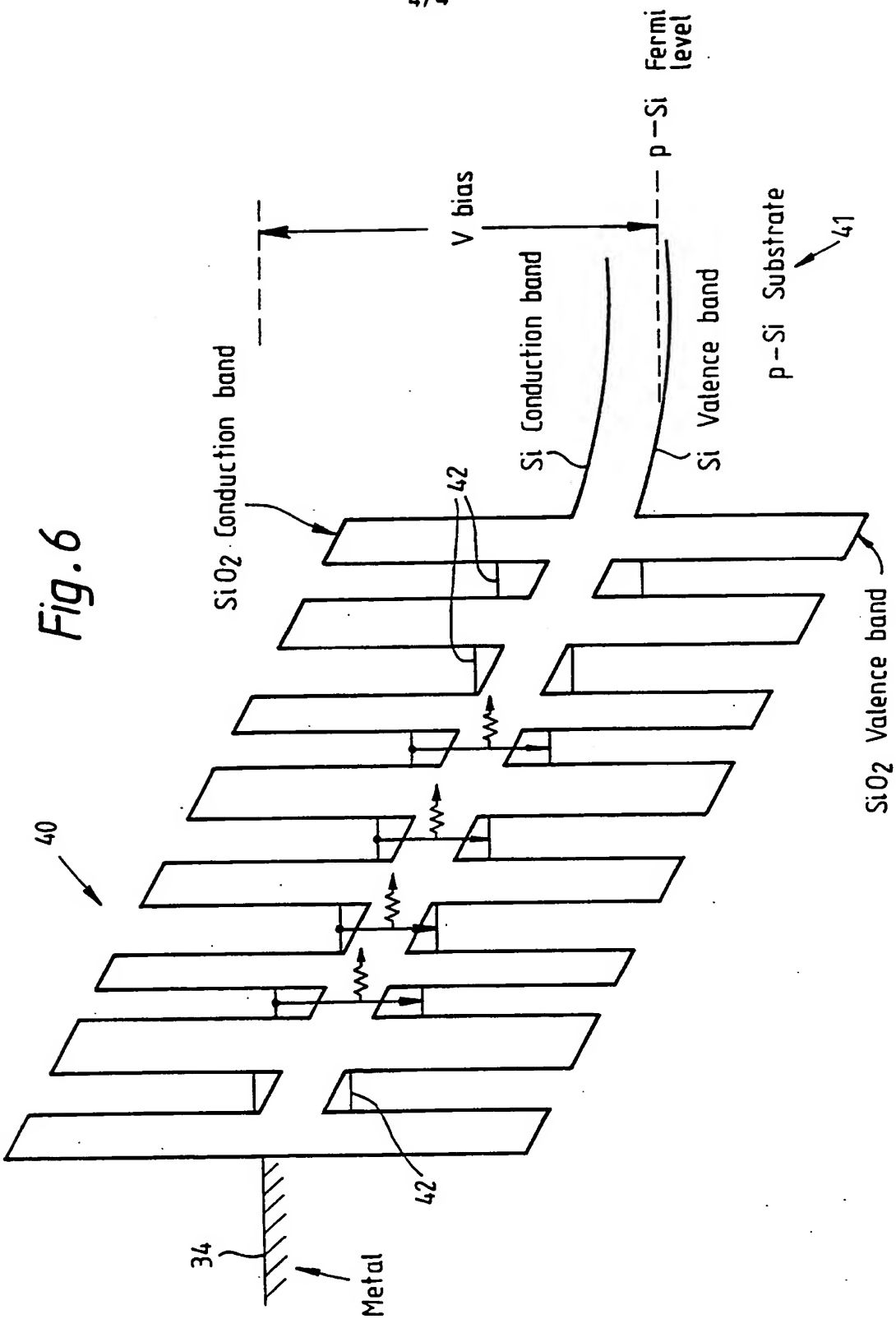


Fig. 6


V bias
p-Si Fermi level
Si Conduction band
Si Valence band
p-Si Substrate
41
SiO_2 Conduction band
42
SiO_2 Valence band
40
42
34
Metal

INTERNATIONAL SEARCH REPORT

International Application No PCT/GB 93/01316

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all)[6]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int.Cl. 5 H01L33/00; H01L21/308

II. FIELDS SEARCHED

Minimum Documentation Searched[7]

Classification System	Classification Symbols
Int.Cl. 5	H01L

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched[8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT[9]

Category °	Citation of Document,[11] with indication, where appropriate, of the relevant passages[12]	Relevant to Claim No.[13]
A	APPLIED PHYSICS LETTERS. vol. 60, no. 3, 20 January 1992, NEW YORK US pages 347 - 349 N. KOSHIDA ET AL. 'Visible electroluminescence from porous silicon' cited in the application see the whole document ---	1,7,14, 21,29,35
A	APPLIED PHYSICS LETTERS. vol. 60, no. 20, 18 May 1992, NEW YORK US pages 2514 - 2516 F. NAMAVAR ET AL. 'Visible electroluminescence from porous silicon np heterojunction diodes' see the whole document --- -/--	1,7,14, 21,29,35

° Special categories of cited documents :[10]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
22 SEPTEMBER 1993	15. 10. 93
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	VISENTIN A.

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

Category °	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No.
A	IEEE ELECTRON DEVICE LETTERS. vol. 12, no. 12, December 1991, NEW YORK US pages 691 - 692 A. RICHTER ET AL. 'Current-induced light emission from a porous silicon device'	
P,X	WO,A,9 219 084 (THE SECRETARY OF STATE FOR DEFENCE) 29 October 1992 see page 7, line 5 - page 8, line 10 see page 15, line 7 - page 16, line 15 see page 18, line 13 - page 20, line 28; figures 1,3	1,7,14, 21,29

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON INTERNATIONAL PATENT APPLICATION NO.

GB 9301316
SA 75523

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report.
The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information. 22/09/93

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO-A-9219084	29-10-92	None	

EPO FORM P0479

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82